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UTILITY PATENT APPLICATION
UNDER 37 CFR 1.53(b)

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Washington, DC 20231
Sir:

Transmitted herewith for filing is the patent application of:

INVENTOR: Eiji HASUNUMA, Hideki GENJO, Shigeru SHIRATAKE, Atsushi HACHISUKA, Koji TANIGUCHI
FOR: SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEROF

Enclosed are:

- ☒ 16 pages of specification, claims, abstract.
- ☒ Declaration and Power of Attorney.
- ☒ Priority Claimed.
- ☒ Certified copy of Japanese Patent Application No. 10-222824
- ☒ 14 sheets of formal drawing.
- ☒ An assignment of the invention to Mitsubishi Denki Kabushiki Kaisha and the assignment recordation fee.
- ☐ An associate power of attorney.
- ☐ A verified statement to establish small entity status under 37 CFR 1.9 and 37 CFR 1.27.
- ☒ Information Disclosure Statement, Form PTO-1449 and reference.
- ☒ Return Receipt Postcard
- ☒ Correspondence Address Change

The filing fee has been calculated as shown below:

	NO. OF CLAIMS		EXTRA CLAIMS	RATE	AMOUNT
Total Claims	7	-20	0	$18.00	$0.00
Independent Claims	2	-3	0	$78.00	$0.00
				Multiple Dependent Claim(s)	$0.00
				Basic Fee	$760.00
				Total of Above Calculations	$760.00
				Less ½ for Small Entity	$0.00
				Assignment & Recording Fee	$40.00
				Total Fee	$800.00

TITLE OF THE INVENTION

Semiconductor Device and Manufacturing Method Thereof

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a semiconductor device and manufacturing method thereof. More specifically, the present invention relates to an improvement of a structure of a semiconductor device allowing improvement in operation characteristic of the semiconductor device, and to manufacturing method thereof.

Description of the Background Art

A structure of a conventional semiconductor device will be described with reference to Fig. 15. Referring to Fig. 15, an element isolating oxide film 2 for defining an active region is provided on a main surface of a p type silicon substrate 1. At a position of a prescribed depth from the main surface of p type silicon substrate 1, there is provided a strip shaped p type isolation region 3. In the active region defined by element isolating oxide film 2, an nMOS (Metal Oxide Semiconductor) 100 is formed.

The nMOS 100 has a gate oxide film 4, a gate electrode 5 and a pair of n type source/drain regions 6. The pair of n type source/drain regions 6 are provided on both sides of gate electrode 5. Upper and side surfaces of gate electrode 5 and surfaces of the pair of n type source/drain regions 6 are covered by an oxide film 7, and oxide film 7 is covered by an interlayer oxide film 8.

A bit line 9 is connected to one of the pair of n type source/drain regions 6. Bit line 9 and interlayer oxide film 8 are covered by an interlayer oxide film 10.

On a lower surface of element isolating oxide film 2, an impurity region 12 is provided connected to the other one of the pair of n type source/drain regions 6. A capacitor 200 is connected to impurity region 12 through a contact hole 10a provided piercing through element isolating oxide film 2.

Capacitor 200 has a storage node (lower electrode) 13 directly connected to impurity region 12, a capacitor dielectric film 14, and a cell

plate (upper electrode) 15. Capacitor dielectric film 14 and cell plate (upper electrode) 15 are provided to extend over interlayer oxide film 10.

A memory cell of a DRAM (Dynamic Random Access Memory) is formed by nMOS 100 and capacitor 200 described above.

In order to meet the demand of reducing the diameter of a contact hole 15a as the semiconductor device has been miniaturized, a framing film 11 of an oxide such as TEOS (Tetra Etyle Ortho Silicate) is provided on a side wall portion of contact hole 15a.

Fig. 16 shows an impurity concentration profile along a cross section taken along the line X of Fig. 15. Referring to Fig. 16, the line A represents concentration of an n type impurity such as phosphorus, and the line B represents concentration of a p type impurity such as boron. Here, a p type isolation region 3 has a depth of at most 0.55μm, and impurity region 12 has a depth of 0.1μm to 0.55μm.

The method of manufacturing the semiconductor device having the above described structure will be described with reference to Figs. 17 to 25.

Referring to Fig. 17, element isolating oxide film 2 is formed on the main surface of p type silicon substrate 1 by LOCOS (Local Oxidation of Silicon) method or trench isolation method. Thereafter, an n type impurity is introduced to the entire main surface of p type silicon substrate 1 to form the strip shaped p type isolation region 3.

Referring to Fig. 18, by photo lithography and etching, gate oxide film 4 and gate electrode 5 having prescribed shapes are formed. Thereafter, referring to Fig. 19, using gate electrode 5 as a mask, an n type impurity is introduced to the main surface of p type silicon substrate 1, to form a pair of n type source/drain regions 6.

Then, referring to Fig. 20, oxide film 7 is formed to cover the upper and side surfaces of gate electrode 5 and the surfaces of the pair of n type source/drain regions 6. Further, interlayer oxide film 8 is formed to cover oxide film 7.

Referring to Fig. 21, a contact hole reaching one of the pair of n type source/drain regions 6 is formed in interlayer oxide film 8, and thereafter bit line 9 formed of a conductive layer connected to one of the pair of n type

source/drain regions 6 is formed.

Thereafter, referring to Fig. 22, interlayer oxide film 10 is formed to cover interlayer oxide film 8 and bit line 9, and by photo lithography and etching, contact hole 10a passing through interlayer oxide film 10, interlayer oxide film 8, oxide film 7 and element isolating oxide film 2 to reach silicon substrate 1 is formed.

Thereafter, referring to Fig. 23, using contact hole 10a, a p type impurity is introduced to p type silicon substrate 1 to form impurity region 12 which is connected to p type isolation region 3 as well as to the other one of the pair of n type source/drain regions 6.

Introduction of the n type impurity at this time is performed with implantation energy of 100keV to 200keV and the dose of $1\times10^{13}cm^{-2}$ to $1\times10^{14}cm^{-2}$. As a result, impurity region 12 comes to have the impurity concentration of about $3\times10^{17}cm^{-3}$ to $3\times10^{18}cm^{-3}$.

Referring to Fig. 24, framing film 11 of an oxide film such as TEOS, is formed to cover an inner portion of contact hole 13a. Then, referring to Fig. 25, framing film 11 on the bottom portion of contact hole 10a and on interlayer oxide film 10 is removed, so as to leave framing film 11 only on the side wall portion of contact hole 10a. Thereafter, in order to remove a natural oxide film formed on the surface of p type silicon substrate 1 exposed at the bottom of contact hole 10a, washing by hydrofluoric acid is performed.

Thereafter, storage node (lower electrode) 13 directly connected to impurity region 12, capacitor dielectric film 14 and cell plate (upper electrode) 15 are formed, and thus a memory cell structure of a DRAM having nMOS 100 and capacitor 200 shown in Fig. 15 is completed.

In the semiconductor device having the above described structure, however, washing with hydrofluoric acid is performed to remove the natural oxide film formed on the p type silicon substrate 1 exposed at the bottom of contact hole 10a, as described above. At this time, framing film 11 of an oxide film such as TEOS provided on the side wall portion of contact hole 10a is etched by the hydrofluoric acid. As a result, framing film 11 is reduced in thickness, resulting in an enlarged diameter of contact

hole 10a.

SUMMARY OF THE INVENTION

Therefore, an object of the present invention is to provide a semiconductor device of which operation characteristic is stabilized by preventing enlargement of the diameter for forming inter connection layers as the semiconductor device is miniaturized, and to provide manufacturing method thereof.

According to the present invention, the semiconductor device includes a semiconductor substrate having a main surface, an element isolating region for defining an element framing region on the main surface of the semiconductor substrate, a strip shaped isolation region having a peak of impurity concentration at a prescribed depth from the main surface of the semiconductor substrate, a connection hole provided piercing through the element isolating region, a hydrofluoric acid resistant side wall film which is not etched by hydrofluoric acid (hereinafter referred to as an anti-HF side wall film) provided to cover the side wall of the connection hole, an interconnection layer provided to fill the connection hole, and an impurity region provided on the semiconductor substrate extending from a lower end portion of the connection hole toward the isolation region.

As described above, an anti-HF side wall film which is not etched by hydrofluoric acid is provided on the side wall of the connection hole, and therefore the thickness of the anti-HF side wall film is not changed even after the step of washing using hydrofluoric acid, during manufacturing of the semiconductor device. As a result, smaller diameter of the connection hole required as the semiconductor device has been miniaturized can effectively be attained.

As a preferable embodiment of the semiconductor device, a nitride film is used as the anti-HF side wall film. More preferably, the impurity region includes a first impurity region provided to connect the interconnection layer to the isolation layer, and a second impurity region provided near a lower end of the connection hole to be connected to the interconnection layer.

As the second impurity region is provided near the lower end of the

connection hole, the semiconductor substrate near the lower end of the connection hole comes to have lower resistance, and hence it becomes possible to improve operation characteristic of the semiconductor device.

In the semiconductor device in accordance with a preferred embodiment, the anti-HF side wall film is either a polysilicon film or an amorphous silicon film.

As the polysilicon film and the amorphous silicon film are conductive, a trap, which is generated at the semiconductor substrate when the first impurity region reaching the isolation region from the lower end of the connection hole is formed, does not present any problem.

The method of manufacturing the semiconductor device in accordance with the present invention includes the following steps.

First, an element isolating region for defining an element framing region is formed in a semiconductor substrate having a main surface. Thereafter, an impurity is introduced to the entire surface of the semiconductor substrate, and a strip-shaped isolation region having peak impurity concentration at a prescribed depth position from the main surface of the semiconductor substrate is formed.

Thereafter, a connection hole piercing through the element isolating region is formed. Then, an anti-HF side wall film which is not etched by hydrofluoric acid, is formed covering the side wall of connection hole at least near the lower end of the connection hole.

Then, an impurity is introduced to the semiconductor substrate through the connection hole, whereby a first impurity region reaching the isolation region from the lower end of the connection hole is formed. Thereafter, inner portion of the connection hole is washed by hydrofluoric acid. Then, an interconnection layer is formed to fill the inside of the connection hole.

As described above, according to the method of manufacturing a semiconductor device of the present invention, even in the step of washing using hydrofluoric acid, thickness of the anti-HF side wall film is unchanged. As a result, the diameter of the connection hole is effectively reduced, as required along with the miniaturization of the semiconductor

device.

Further, in a preferred embodiment of the manufacturing method of the semiconductor device, in the step of forming the anti-HF side wall film, either polysilicon film or an amorphous silicon film is formed. When such a film is used, the thickness of the anti-HF side wall film is unchanged even in the step of washing using hydrofluoric acid. Further, since these films are conductive, the trap generated in the semiconductor substrate when the first impurity region reaching the isolation region from the lower end of the connection hole is formed does not present any problem.

In the preferred embodiment, in the step of forming the anti-HF side wall film, a nitride film is formed, and before the anti-HF side wall film is formed on the side wall of the connection hole, an impurity is introduced to the semiconductor substrate through the connection hole, whereby a second impurity region is formed near the lower end of the connection hole. The thickness of the anti-HF side wall film is unchanged in the step of washing using hydrofluoric acid also in this example using nitride film.

As to the trap generated in the semiconductor substrate when the first impurity region is formed from the lower end of the connection hole to the isolation region, the trap does not present any problem, as the second impurity region is formed near the lower end of the connection hole. Further, as the second impurity region is provided near the lower end of the connection hole, the semiconductor substrate near the lower end of the connection hole comes to have lower resistance, and hence operation characteristic of the semiconductor device can be improved.

The foregoing and other objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a cross section schematically showing a structure of a semiconductor device in accordance with a first embodiment.

Fig. 2 shows an impurity concentration profile of a cross section taken along the line X of Fig. 1.

Figs. 3 to 12 are cross sectional views showing the first to tenth steps of the method of manufacturing the semiconductor device in accordance with a first embodiment.

Fig. 13 is a cross sectional view schematically showing the structure of the semiconductor device in accordance with a second embodiment.

Fig. 14 is a cross sectional view schematically showing a structure of a semiconductor device in accordance with a third embodiment.

Fig. 15 is a cross sectional view schematically showing a structure of a semiconductor device in accordance with the prior art.

Fig. 16 shows an impurity concentration profile of a cross section taken along the line X in Fig. 15.

Figs. 17 to 25 are cross sectional view showing the first to ninth steps of a method of manufacturing the semiconductor device in accordance with the prior art.

Fig. 26 is a schematic diagram showing the problems of the semiconductor device and the manufacturing method thereof in accordance with the prior art.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Embodiment of the semiconductor device and manufacturing method thereof in accordance with the present invention will be described in the following with reference to the figures.

First Embodiment

The semiconductor device and manufacturing method thereof in accordance with the first embodiment will be described in the following with reference to the figures.

Referring to Fig. 1, on a main surface of a p type silicon substrate 1, an element isolating oxide film 2 of a silicon oxide film, for example, for defining an active region is provided. At a prescribed depth position from the main surface of p type silicon substrate 1, a strip shaped p type isolation region 3 is provided. In the active region defined by element isolating oxide film 2, an nMOS 100 is formed.

The nMOS 100 has a gate oxide film 4, a gate electrode 5 and a pair of n type source/drain regions 6. The pair of n type source/drain regions 6

are provided on both sides of gate electrode 5. The upper and side surfaces of gate electrode 5 and surfaces of the pair of n type source/drain region 6 are covered by an oxide film 7 and oxide film 7 is covered by an interlayer oxide film 8.

A bit line 9 is connected to one of the pair of n type source/drain regions 6. Bit line 9 and interlayer oxide film 8 are covered by an interlayer oxide film 10.

In silicon substrate 1 near the lower end portion of contact hole 10a, there are provided a first impurity region 52 reaching the p type isolation region 3 and a second impurity region 50 connected to the other one of the pair of n type source/drain regions 6. To the first impurity region 52, a capacitor 200 as an interconnection layer is connected through a contact hole 10a provided passing through element isolating oxide film 2.

The first impurity region 52 is formed to reach p type isolation region 3 here, in order to lower impurity concentration of p type isolation region 3 by introducing an n type impurity, which is opposite to p type isolation region 3 into silicon substrate 1.

As the impurity concentration of p type isolation region is decreased, it becomes possible to relax electric field in the X direction from the lower end portion of contact hole 10a to p type isolation region 3. As a result, the leakage current through the X direction of the charges from storage node 13 (which will described later) can be reduced, and hence it becomes possible to decrease impurity concentration of a pn junction formed by p type isolation region 3 and n type source/drain region 6.

Capacitor 200 includes a storage node (lower electrode) 13 directly connected to first impurity region 52, a capacitor dielectric film 14 and a cell plate (upper electrode) 15. Capacitor dielectric film 14 and cell plate (upper electrode) 15 are provided to extend over interlayer oxide film 10.

The DRAM memory cell is formed by nMOS 100 and capacitor 200 described above.

In order to meet the demand of reduced diameter of the contact hole 10a along with miniaturization of the semiconductor device, an anti-HF side wall film 51 which is not etched by hydrofluoric acid, formed of an

isolating film such as a nitride film is provided.

Fig. 2 shows an impurity concentration profile of the cross section taken along the line X of Fig. 1. Referring to Fig. 2, the line A represents concentration of the n type impurity such as phosphorus, and the line B represents concentration of the p type impurity such as boron. Here, p type isolation region 3 corresponds to the region of which depth is at most 0.55μm, the first impurity region 52 corresponds to the region at the depth of 0.1μm to 0.55μm, and the second impurity region 50 corresponds to the region having the depths of 0.1μm to 0.25μm, overlapped with the first impurity region 52.

The method of manufacturing the semiconductor device having the above described structure will be described with reference to Figs. 3 to 12.

Referring to Fig. 3, element isolating oxide film 2 is formed by LOCOS (Local Oxidation of Silicon) method or trench isolation method on the main surface of p type silicon substrate 1. Thereafter, an n type impurity is introduced to the entire main surface of p type silicon substrate 1, to form a strip shaped p type isolation region 3. The impurity concentration of p type isolation region 3 is set to be $1\times10^{17}cm^{-3}$ to $5\times10^{17}cm^{-3}$.

Referring to Fig. 4, thereafter, a gate oxide film 4 and a gate electrode 5 having prescribed shapes are formed by photo lithography and etching. Then, referring to Fig. 5, using a gate electrode 5 as a mask, an n type impurity is introduced to the main surface of p type silicon substrate 1, to form the pair of n type source/drain regions 6. The impurity concentration of the pair of n type source/drain regions 6 is set to be $5\times10^{17}cm^{-3}$ to $1\times10^{18}cm^{-3}$.

Thereafter, an oxide film 7 is formed to cover the upper and side surfaces of gate electrode 5 and the surfaces of the pair of n type source/drain regions 6, as shown in Fig. 6. Thereafter, an interlayer oxide film 8 is formed to cover oxide film 7.

Then, referring to Fig. 7, a contact hole reaching one of the pair of n type source/drain regions 6 is formed through oxide film 7 and interlayer oxide film 8, and a bit line 9 of a conductive layer such as aluminum is

formed to be connected to one of the pair of n type source/drain regions 6.

Then, referring to Fig. 8, an interlayer oxide film 10 is formed to cover interlayer oxide film 8 and bit line 9, and thereafter, using photo lithography and etching, a contact hole 10a passing through interlayer oxide film 10, interlayer oxide film 8, oxide film 7 and element isolating oxide film 2 to reach silicon substrate 1 is formed by dry etching. The condition for dry etching is 41mTorr, 1700W, C_4F_8 : 10sccm, CO : 50sccm, Ar : 250sccm, and O_2 : 5sccm.

Then, referring to Fig. 9, an n type impurity (for example, phosphorus) is introduced to p type silicon substrate 1 through contact hole 10a, to form a second impurity region 50 connected to the other one of the pair of n type source/drain regions 6.

The condition for n type impurity introduction at this time is implantation energy of 20keV to 120keV and the dose of $8\times10^{12}cm^{-2}$ to $8\times10^{13}cm^{-2}$. As a result, the second impurity region 50 comes to have the impurity concentration of about $2\times10^{17}cm^{-3}$ to about $2\times10^{18}cm^{-3}$.

Then, referring to Fig. 10, an anti-HF side wall film 51 of an oxide film is formed to cover an inner portion of contact hole 10a. Then, referring to Fig. 11, anti-HF side wall film 51 on the bottom portion of contact hole 10a and on interlayer oxide film 10 is removed by dry etching, so that anti-HF side wall film 51 is left only on the side wall portions of contact hole 10a. The condition for dry etching is 60mTorr, 700W, CHF_3 : 50sccm, and Ar : 100sccm.

Thereafter, in order to remove a natural oxide film formed on the surface of p type silicon substrate 1 exposed at the bottom portion of contact hole 10a, washing with hydrofluoric acid is conducted.

Referring to Fig. 12, an n type impurity region (for example, phosphorus) is introduced to p type silicon substrate 1 through contact hole 10a, and a first impurity region 52 connected to p type isolation region 3 is formed.

The condition for n type impurity implantation at this time is implantation energy of 80keV to 180keV and the dose of $8\times10^{12}cm^{-2}$ to $8\times10^{13}cm^{-3}$. As a result, the first impurity region 52 comes to have the

impurity concentration of about $2\times10^{17}cm^{-3}$ to about $2\times10^{13}cm^{-3}$.

Then, a storage node (lower electrode) 13 directly connected to the first impurity region 52, a capacitor dielectric film 14 and a cell plate (upper electrode) 15 are formed, and thus the DRAM memory cell structure in accordance with the embodiment having nMOS 100 and capacitor 200 shown in Fig. 1 is complete.

According to the semiconductor device and manufacturing method thereof in accordance with the present embodiment, even when a nitride film is used, the nitride film used as the anti-HF side wall film 51, and therefore thickness of anti-HF side wall film 51 is unchanged in the step of washing using hydrofluoric acid. Therefore, refresh characteristic of the DRAM can be improved.

As to the trap generated in the silicon substrate 1 when the first impurity region 52 reaching isolation region 3 from the lower end of contact hole 10a, the trap does not present any problem, as the second impurity region 50 is formed in silicon substrate 1 near the lower end of contact hole 10a.

Further, as the second impurity region 50 is provided in silicon substrate 1 near the lower end of contact hole 10a, silicon substrate 1 near the lower end of contact hole 10a comes to have lower resistance, which allows improved write characteristic of the DRAM.

Second Embodiment

The semiconductor device and manufacturing method thereof in accordance with the second embodiment will be described with reference to the Fig. 13.

Referring to Fig. 13, the semiconductor device of the present embodiment is basically the same in structure as the semiconductor device in accordance with the first embodiment described above. Therefore, only the difference will be described in detail.

Portions corresponding to those of the semiconductor device in accordance with the first embodiment are denoted by the same reference characters. In the semiconductor device according to the present embodiment, in place of the anti-HF side wall film 51 formed of a nitride

film in the first embodiment, an anti-HF side wall film 53 formed of a conductive film such as polysilicon or amorphous silicon is formed on the side wall portion of contact hole 10a.

Even when the anti-HF side wall film 53 which is a conductive film is used, the thickness of the anti-HF side wall film is unchanged in the step of washing using hydrofluoric acid. Therefore, it becomes possible to improve refresh characteristic of the DRAM.

Further, anti-HF side wall film 53 is formed of a conductive film, the trap generated in silicon substrate 1 when the first impurity region 52 reaching isolation region 3 from the lower end of contact hole 10a described in the first embodiment is formed does not present any problem. As a result, it is not necessary in the present embodiment to form the second impurity region 50 in silicon substrate 1 near the lower end of contact hole 10a.

Third Embodiment

The semiconductor device in accordance with the third embodiment will be described with reference to the Fig. 14.

Referring to Fig. 14, the semiconductor device in accordance with the present embodiment is basically the same in structure as the semiconductor device in accordance with the first embodiment described above. Therefore, only the difference will be described in detail. Portions corresponding to those of the semiconductor device in accordance with the first embodiment will be denoted by the same reference characters.

In the semiconductor device in accordance with the present embodiment, the anti-HF side wall film 51 formed of a nitride film in the first embodiment is formed only in the vicinity of a lower end portion of the side wall of contact hole 10a. Formation of anti-HF side wall film 51 with reduced height is possible by appropriately selecting the condition of dry etching in the step of dry etching shown in Fig. 11 of the first embodiment.

Similar function and effect as in the first embodiment can be obtained in the semiconductor device in accordance with the third embodiment.

The embodiments described above are exemplary and not limiting.

Though an insulating film of a nitride film, a polysilicon or an amorphous conductive film has been described as the anti-HF side wall film, any material may be used provided that it has slower etching rate than an oxide film such as TEOS with respect to hydrofluoric acid. If the material is an insulator, the structure similar to the first embodiment may be used and if the material is a conductor, a structure similar to that of the second embodiment may be used, to obtain similar function and effects as in the first and second embodiments.

Although the present invention has been described and illustrated in detail, it is clearly understood that the same is by way of illustration and example only and is not to be taken by way of limitation, the spirit and scope of the present invention being limited only by the terms of the appended claims.

WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a semiconductor substrate having a main surface;

an element isolation region for defining an element forming region on the main surface of said semiconductor substrate;

an isolation region provided in a strip-shape and having a peak impurity concentration at a prescribed depth position from the main surface of said semiconductor substrate;

a connection hole provided piercing through said element isolating region;

an anti-HF side wall film not etched by hydrofluoric acid, provided to cover a side wall of said connection hole at least near a lower end of said connection hole;

an interconnection layer provided to fill an inner portion of said connection hole; and

an impurity region provided in said semiconductor substrate extending from the lower end of said connection hole to said isolation region.

2. The semiconductor device according to claim 1, wherein said anti-HF side wall film is a nitride film.

3. The semiconductor device according to claim 2, wherein

said impurity region includes a first impurity region provided to connected said interconnection layer to said isolation region, and a second impurity region provided near the lower end of said connection hole and connected to said interconnection layer.

4. The semiconductor device according to claim 1, wherein said anti-HF side wall film is either a polysilicon film or an amorphous silicon film.

5. A method of manufacturing a semiconductor device,

comprising the steps of:

forming an element isolating region for defining an element forming region on a semiconductor substrate having a main surface;

introducing an impurity to an entire surface of said semiconductor substrate to form a strip-shaped isolation region having a peak impurity concentration at a prescribed depth position from the main surface of said semiconductor substrate;

forming a connection hole piercing through said element isolating region;

forming an anti-HF side wall film not etched by hydrofluoric acid, provided to cover a side wall of said connection hole at least near a lower end of said connection hole;

introducing an impurity to said semiconductor substrate through said connection hole to form a first impurity region reaching from the lower end of said connection hole to said isolation region;

washing an inner portion of said connection hole by hydrofluoric acid; and

forming an interconnection layer to fill the inner portion of said connection hole.

6. The method of manufacturing a semiconductor device according to claim 5, wherein a polysilicon film or an amorphous silicon film is formed in said step of forming the anti-HF side wall film.

7. The method of manufacturing a semiconductor device according to claim 5, wherein said step of forming said anti-HF side wall film includes the steps of forming a nitride film, and before said anti-HF side wall film is formed on the side wall of said connection hole, introducing an impurity to said semiconductor substrate through said connection hole to form a second impurity region near the lower end of said connection hole.

ABSTRACT OF THE DISCLOSURE

In the semiconductor device, in order to meet the demand of reduced diameter of a contact hole along with the miniaturization of the semiconductor device, an anti-HF side wall film which is not etched by a hydrofluoric acid, formed of an isolating film such as nitride film, is provided on the side wall of contact hole. Further, a second impurity region which is connected to one of the pair of n type source/drain regions and a first impurity region reaching a p type isolation region are provided in silicon substrate 1 near the lower end of contact hole. Because of this structure, it becomes possible to prevent expansion of the diameter for forming the interconnection layer, as desired in the miniaturized semiconductor device, and therefore a semiconductor device and manufacturing method thereof which stabilize operation characteristic of the semiconductor device can be provided.

FIG. 1

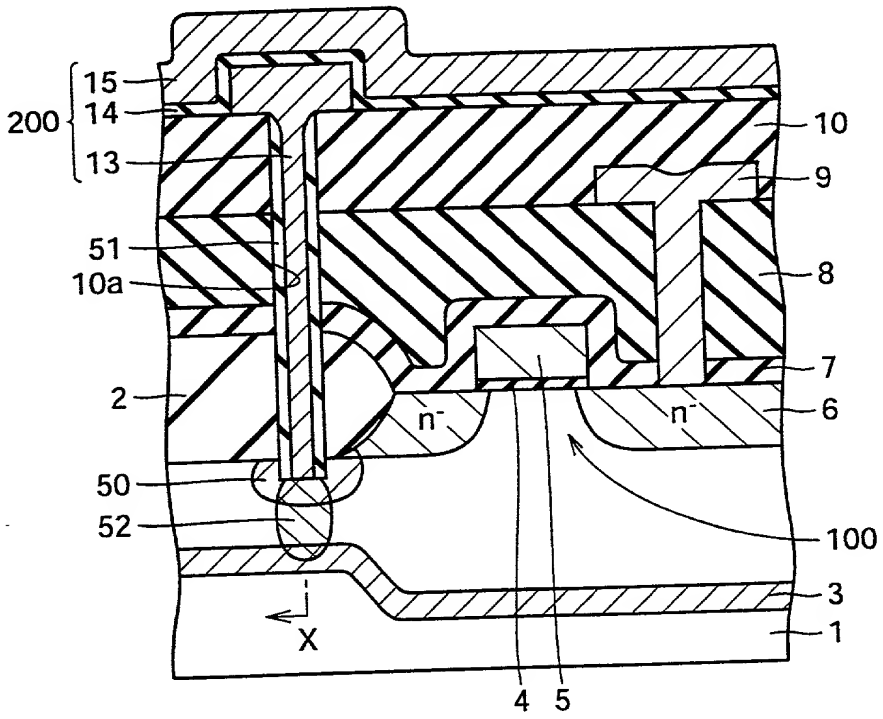


FIG. 2

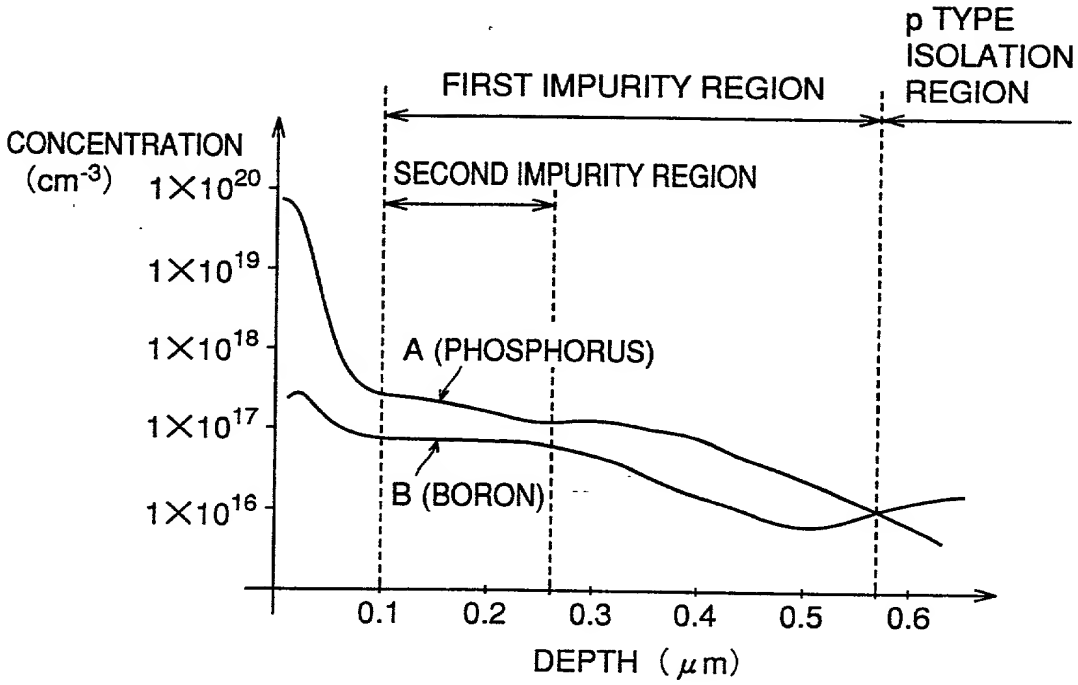

p TYPE
ISOLATION
REGION
FIRST IMPURITY REGION
SECOND IMPURITY REGION
CONCENTRATION
(cm-3)
1×10^20
1×10^19
1×10^18
1×10^17
1×10^16
A (PHOSPHORUS)
B (BORON)
0.1
0.2
0.3
0.4
0.5
0.6
DEPTH (μm)

FIG. 3

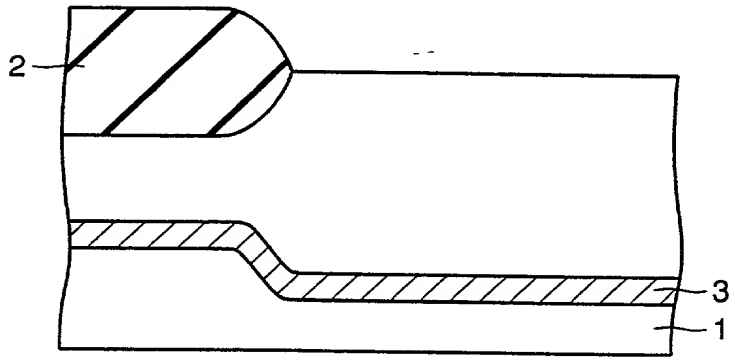

2
3
1

FIG. 4

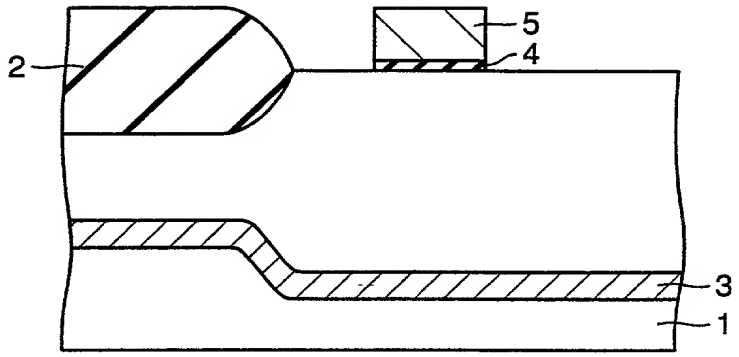


FIG. 5

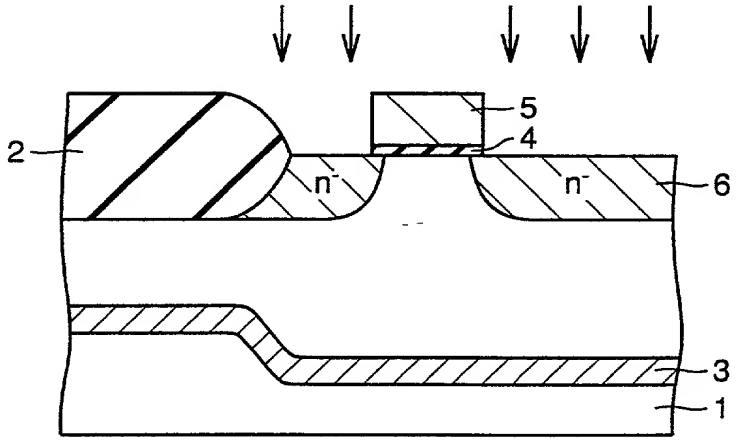


FIG. 6

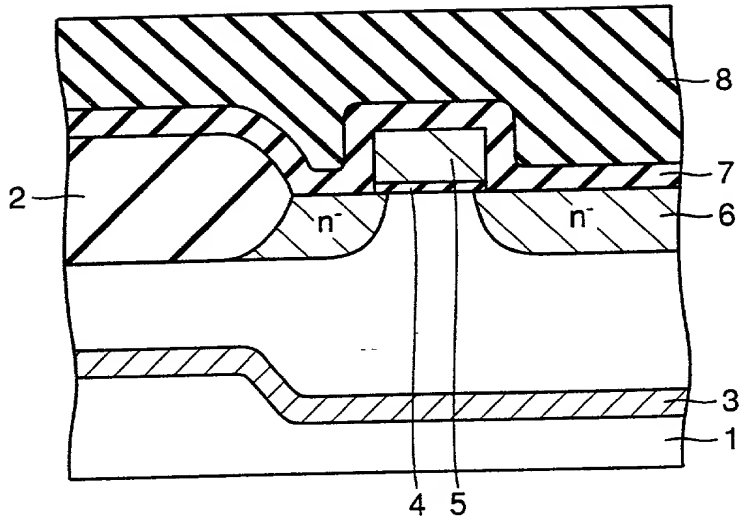


FIG. 7

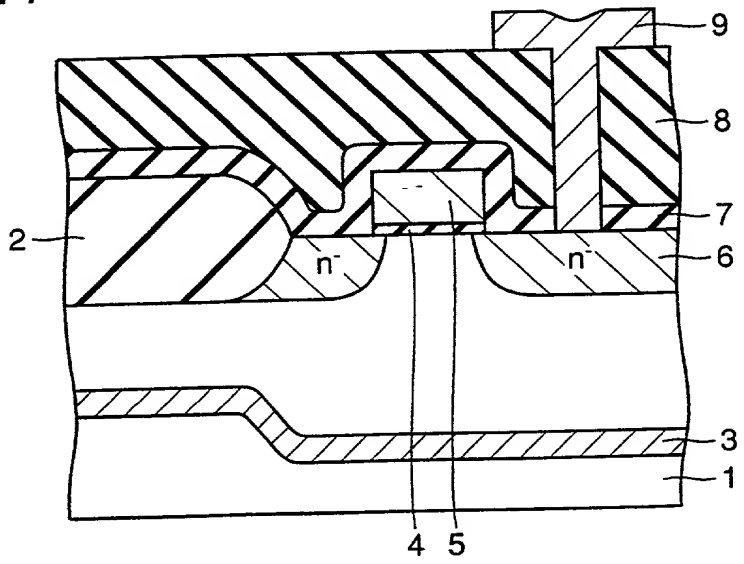


FIG. 8

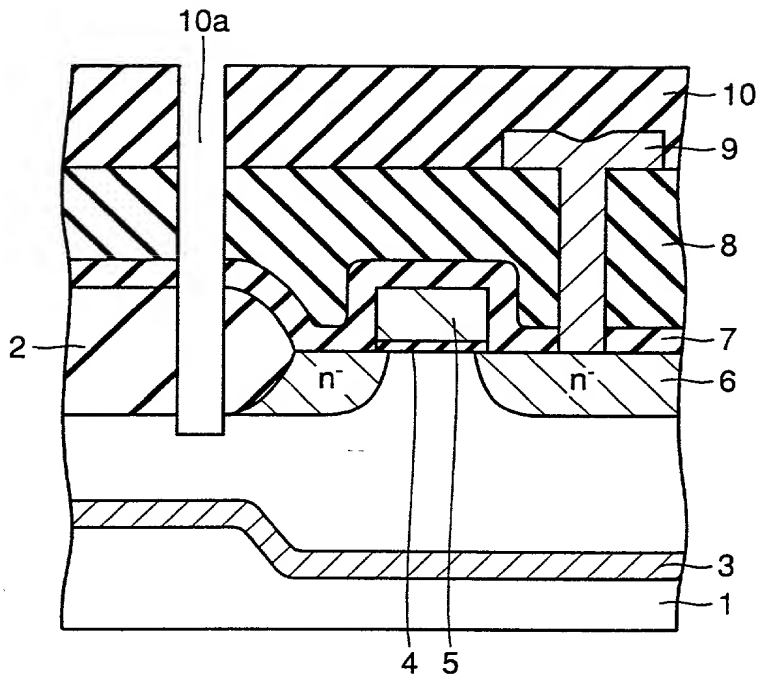


FIG. 9

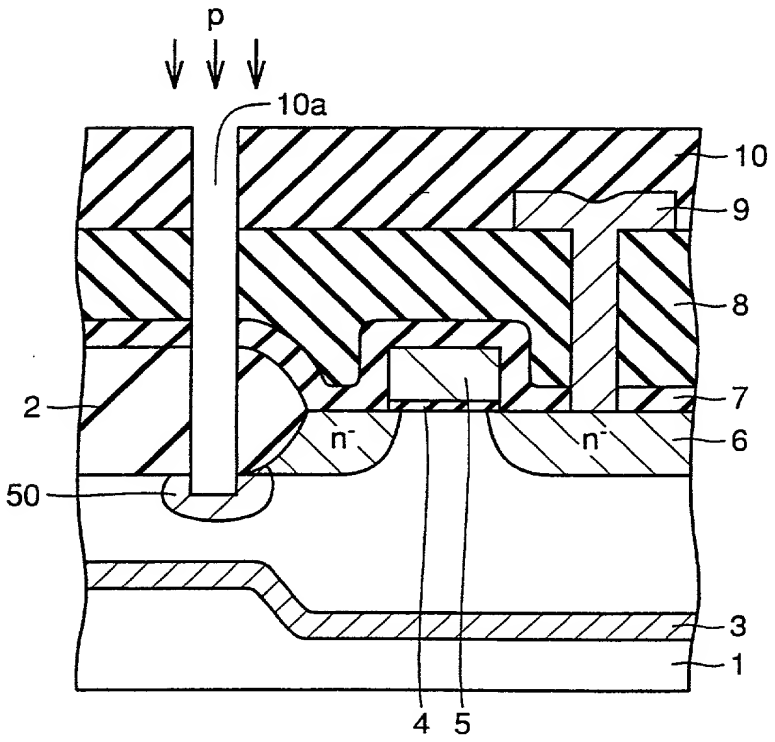


FIG. 10

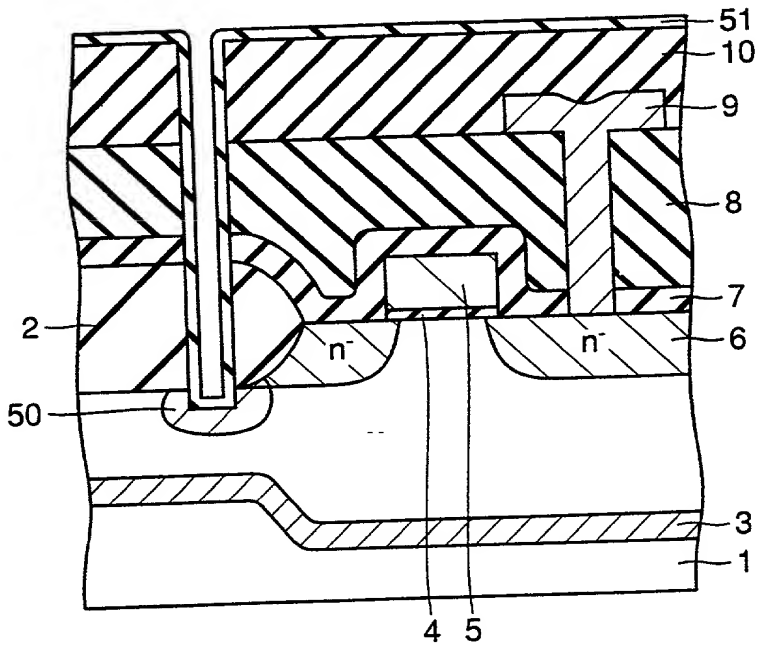


FIG. 11

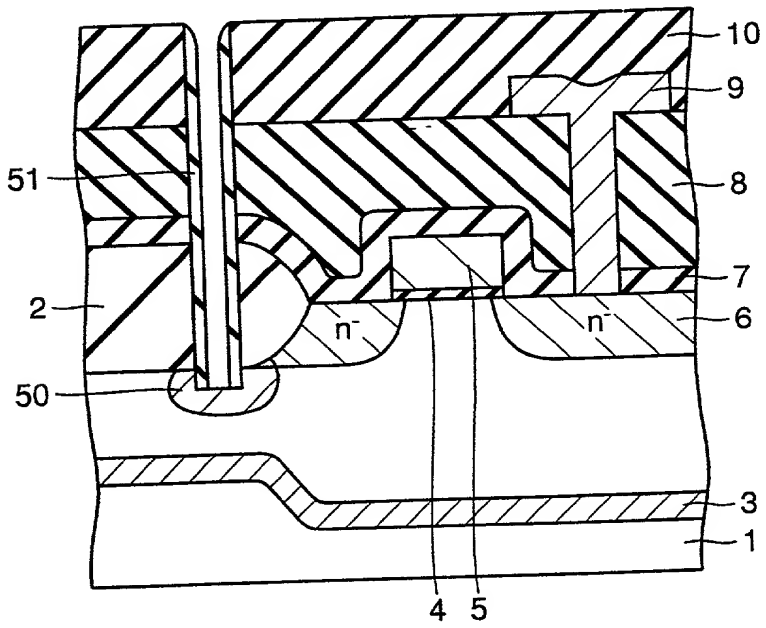


FIG. 12

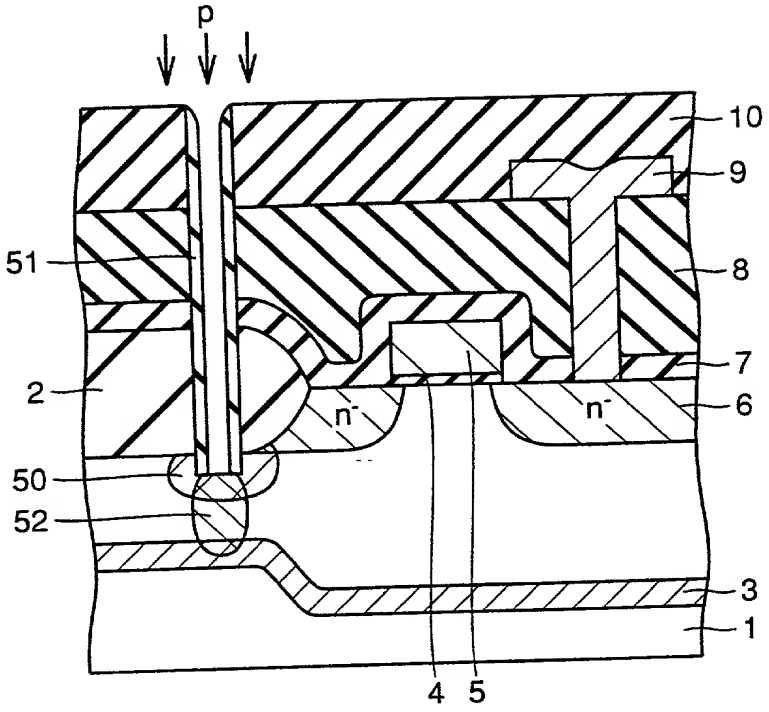


FIG. 13

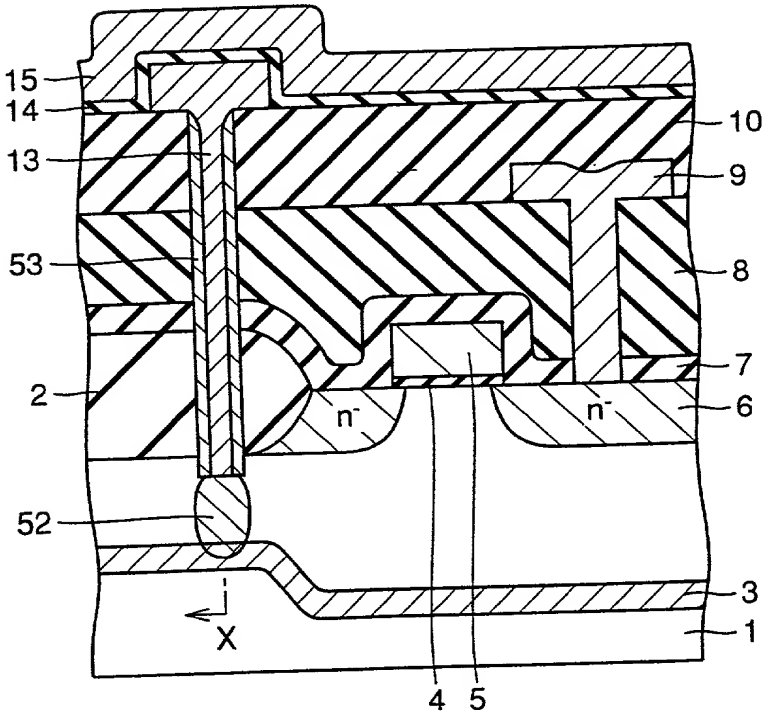


FIG. 14

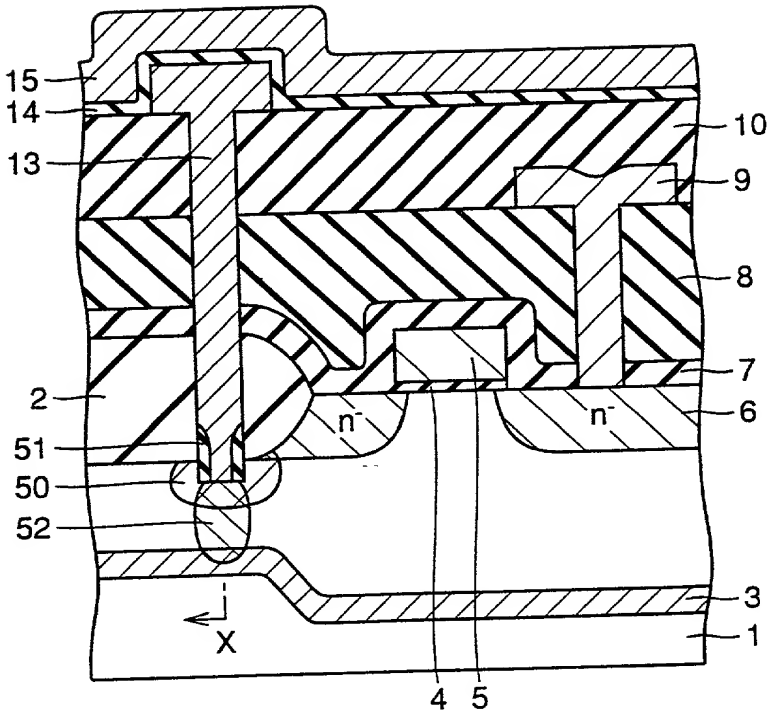


FIG. 15 PRIOR ART

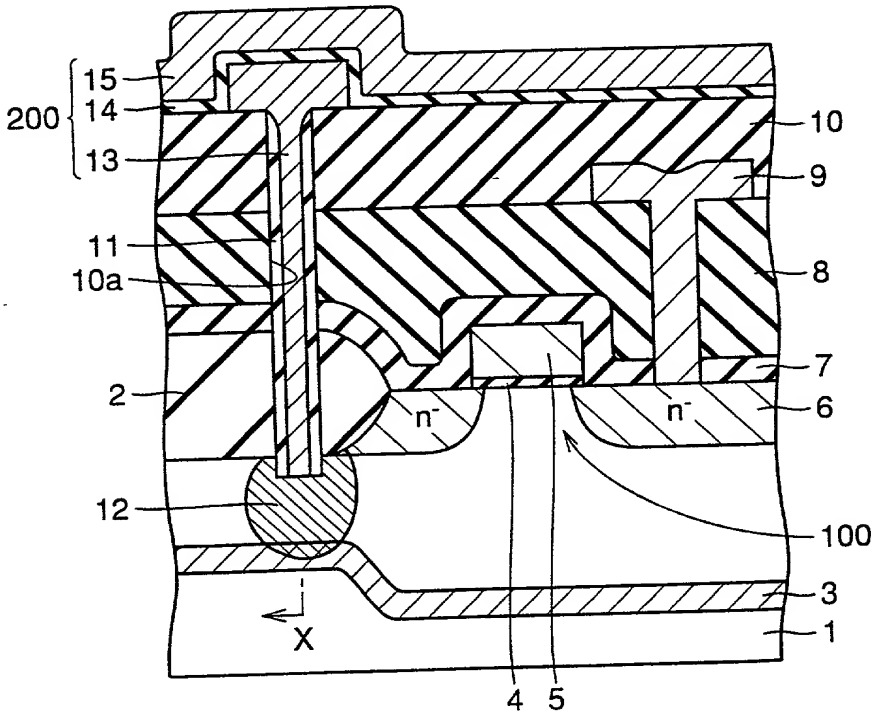


FIG. 16 PRIOR ART

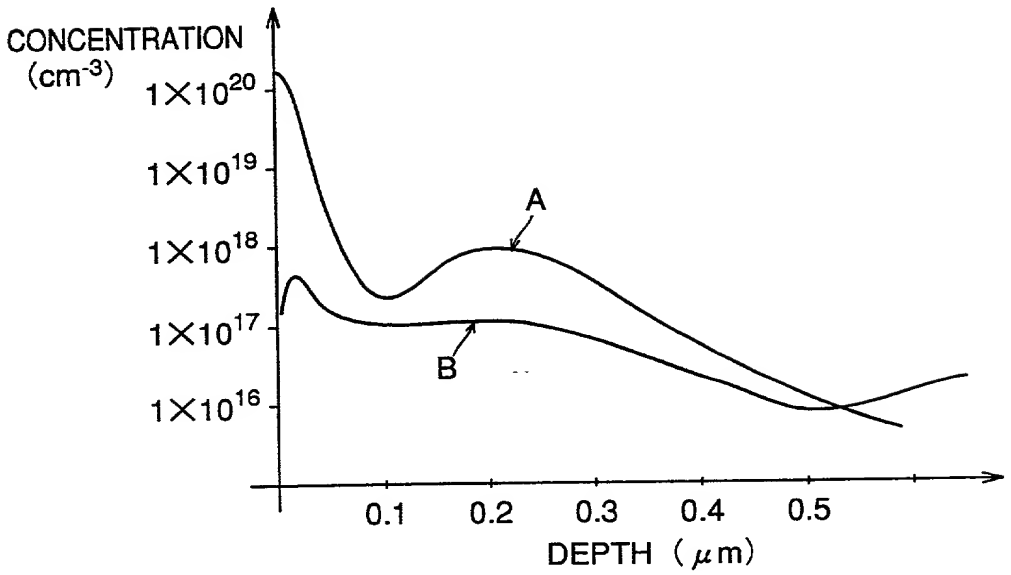


FIG. 17 PRIOR ART

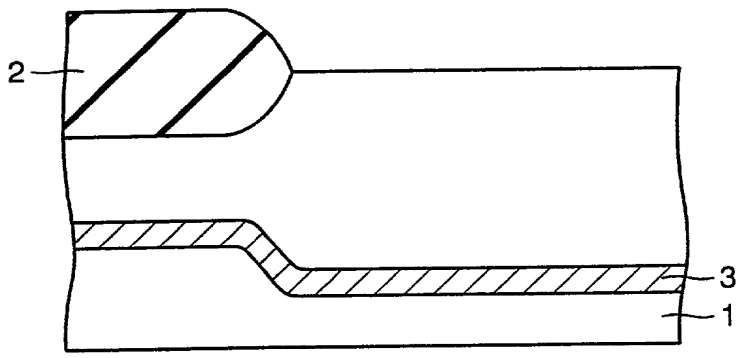


FIG. 20 PRIOR ART

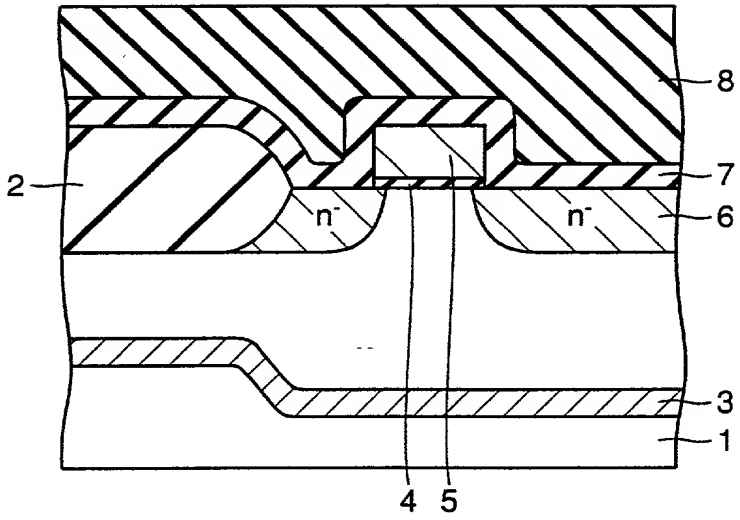


FIG. 21 PRIOR ART

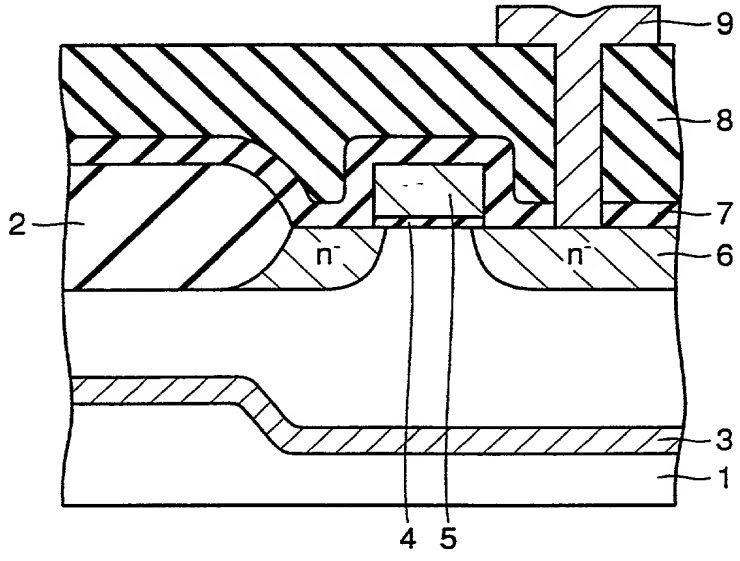


FIG. 22 PRIOR ART

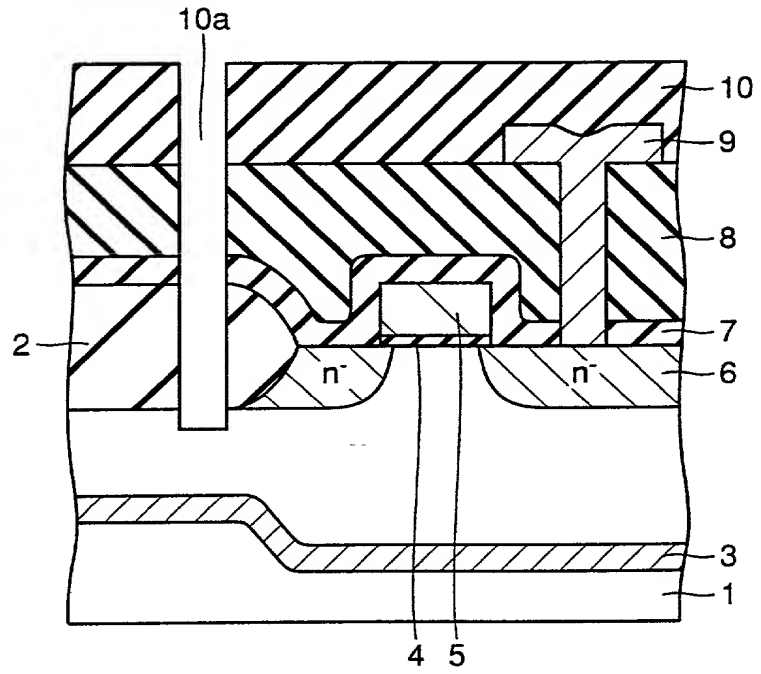


FIG. 23 PRIOR ART

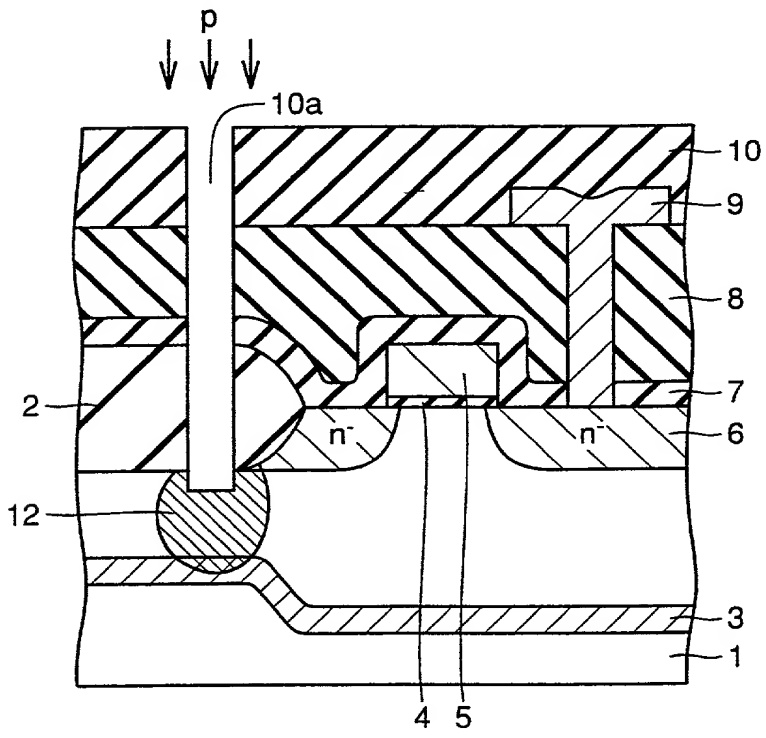


FIG. 18 PRIOR ART

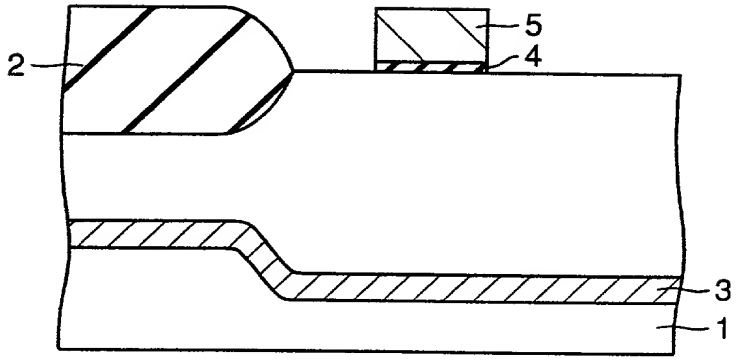


FIG. 19 PRIOR ART

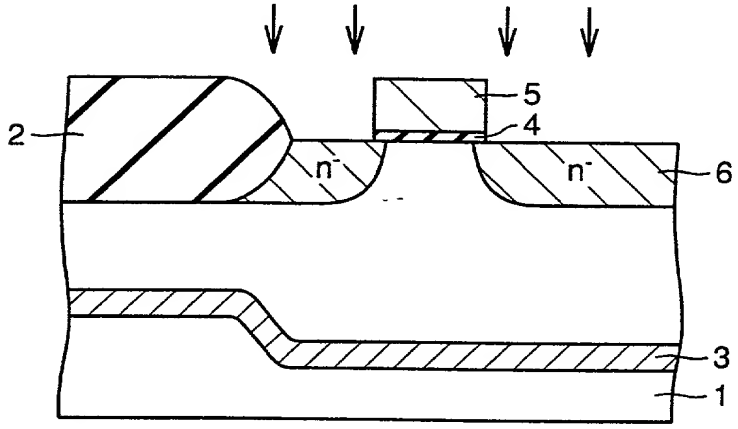
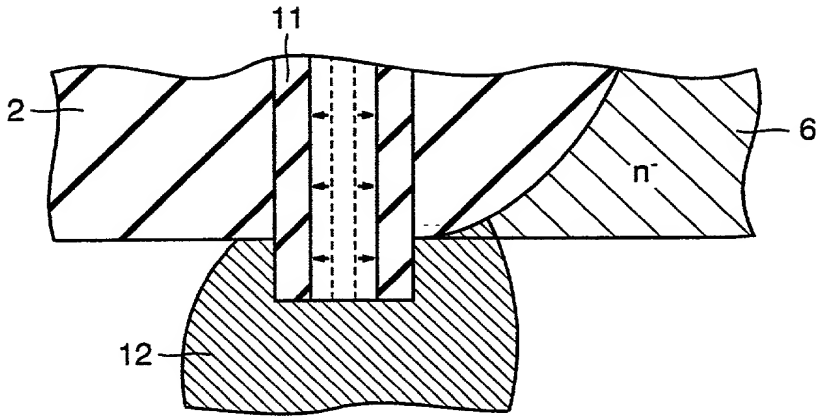


FIG. 26 PRIOR ART



Declaration and Power of Attorney For Patent Application

特許出願宣言書

Japanese Language Declaration

私は、下欄に氏名を記載した発明者として、以下のとおり宣言する：

As a below named inventor, I hereby declare that:

私の住所、郵便の宛先および国籍は、下欄に氏名に続いて記載したとおりであり、

My residence, post office address and citizenship are as stated below next to my name,

名称の発明に関し、請求の範囲に記載した特許を求める主題の本来の、最初にして唯一の発明者である（一人の氏名のみが下欄に記載されている場合）か、もしくは本来の、最初にして共同の発明者である（複数の氏名が下欄に記載されている場合）と信じ、

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

その明細書を
（該当する方に印を付す）

the specification of which
(check one)

☐ ここに添付する。

☒ is attached hereto.

☐ _____ 日に出願番号

☐ was filed on _____ as Application Serial No. _____

第 _____ 号として提出し、

_____ 日に補正した。
（該当する場合）

and was amended on _____ (if applicable)

私は、前記のとおり補正した請求の範囲を含む前記明細書の内容を検討し、理解したことを陳述する。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第37部第1章第56条（a）項に従い、本願の審査に所要の情報を開示すべき義務を有することを認める。

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

Japanese Language Declaration

私は、合衆国法典第35部第119 条にもとづく下記の外国特許出願または発明者証出願の外国優先権利益を主張し、さらに優先権の主張に係わる基礎出願の出願日前の出願日を有する外国特許出願または発明者証出願を以下に明記する：

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior foreign applications
先の外国出願

(Number) (番 号)	(Country) (国 名)	(Day/Month/Year Filed) (出願の年月日)	Priority claimed 優先権の主張 Yes あり	No なし
10-222824(P)	Japan	6/August/1998	[X]	[ ]
			[ ]	[ ]
			[ ]	[ ]

私は、合衆国法典第35部第120 条にもとづく下記の合衆国特許出願の利益を主張し、本願の請求の範囲各項に記載の主題が合衆国法典第35部第112 条第１項に規定の態様で先の合衆国出願に開示されていない限度において、先の出願の出願日と本願の国内出願日またはＰＣＴ国際出願日の間に公表された連邦規則法典第37部第１章第56条（ａ）項に記載の所要の情報を開示すべき義務を有することを認める：

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.) (出願番号)	(Filing Date) (出願日)	(現 況) (特許済み、係属中、放棄済み)	(Status) (patented, pending, abandoned)

私は、ここに自己の知識にもとづいて行った陳述がすべて真実であり、自己の有する情報および信ずるところに従って行った陳述が真実であると信じ、さらに故意に虚偽の陳述等を行った場合、合衆国法典第18部第1001条により、罰金もしくは禁錮に処せられるか、またはこれらの刑が併科され、またかかる故意による虚偽の陳述が本願ないし本願に対して付与される特許の有効性を損うことがあることを認識して、以上の陳述を行ったことを宣言する。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Japanese Language Declaration

委任状：私は、下記発明者として、以下の代理人をここに選任し、本願の手続を遂行すること並びにこれに関する一切の行為を特許商標庁に対して行うことを委任する。
（代理人氏名および登録番号を明記のこと）

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. (*list name and registration number*)

Stanislaus Aksman, Reg. No. 28,562; Edward A. Becker, Reg. No. 37,777; Stephen A. Becker, Reg. No. 26,527; William H. Beha, Reg. No. 38,038; John G. Bisbikis, Reg. No. 37,095; Kenneth L. Cage, Reg. No. 26,151; Stephen C. Carlson, Reg. No. 39,929; Paul Devinsky, Reg. No. 28,553; Laura A. Donnelly, Reg. No. 38,435; Margaret M. Duncan, Reg. No. 30,879; Brian E. Ferguson, Reg. No. 36,801; Michael F. Fogarty, Reg. No. 36,139; Wilhelm F. Gadiano, Reg. No. 37,136; Keith E. George, Reg. No. 34,111; John A. Hankins, Reg. No. 32,029; Thomas A. Jolly, Reg. No. 39,241; Eric J. Kraus, Reg. No. 36,190; Edward E. Kubasiewicz, Reg. No. 30,020; Robert E. LeBlanc, Reg. No. 17,219; Jack Q. Lever, Reg. No. 28,149; Raphael V. Lupo, Reg. No. 28,363; Christine F. Martin, Reg. No. 39.762; Michael E. McCabe, Jr., Reg. No. 37,182; James H. Meadows, Reg. No. 33,965; Michael A. Messina, Reg. No. 33,424; Joseph H. Paquin, Jr., Reg. No. 31,647; Craig L. Plastrik, Reg. No. 41,254; Robert L. Price, Reg. No. 22,685; Paul A. Roberts, Reg. No. 40,289; Gene Z. Rubinson, Reg. No. 33,351; Joy Ann G. Serauskas, Reg. No. 27,952; Michele M. Schafer, Reg. No. 34,717; David J. Serbin, Reg. No. 30,589; Glenn Snyder, Reg. No. 41,428; Arthur J. Steiner, Reg. No. 26,106; David L. Stewart, Reg. No. 37,578; Leonid D. Thenor, Reg. No. 39,397; Keith J. Townsend, Reg. No. 40,358; Leon R. Turkevich, Reg. No. 34,035; Christopher D. Ward, Reg. No. 41,367; Damian G. Wasserbauer, Reg. No. 34,749; Edward J. Wise, Reg. No. 34,523; Alexander V. Yampolsky, Reg. No. 36,324; and Robert W. Zelnick, Reg. No. 36,976

書類の送付先：

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99 Canal Center Plaza, Suite 300
Alexandria, Virginia 22314

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Direct Telephone Calls to: (*name and telephone number*)

Stephen A. Becker
(202)756-8600

唯一のまたは第一の発明者の氏名	Full name of sole or first inventor Eiji HASUNUMA
同発明者の署名　日付	Inventor's signature　Date Eiji Hasunuma　November 18, 1998
住所	Residence Hyogo, Japan
国籍	Citizenship Japanese
郵便の宛先	Post Office Address c/o Mitsubishi Denki Kabushiki Kaisha
	2-3, Marunouchi 2-chome, Chiyoda-ku, TOKYO 100-8310 JAPAN
第２の共同発明者の氏名（該当する場合）	Full name of second joint inventor, if any Hideki GENJO
同第２発明者の署名　日付	Second inventor's signature　Date Hideki Genjo　November 18, 1998
住所	Residence Hyogo, Japan
国籍	Citizenship Japanese
郵便の宛先	Post Office Address c/o Mitsubishi Denki Kabushiki Kaisha
	2-3, Marunouchi 2-chome, Chiyoda-ku, TOKYO 100-8310 JAPAN

（第六またはそれ以降の共同発明者に対しても同様な情報および署名を提供すること。）

(Supply similar information and signature for third and subsequent joint inventors.)

Japanese Language Declaration

第3の共同発明者の氏名(該当する場合)	Full name of third joint inventor, if any Shigeru SHIRATAKE
同第3共同発明者の署名　日付	Third Inventor's signature　Date Shigeru Shiratake　November 18, 1998
住所	Residence Hyogo, Japan
国籍	Citizenship Japanese
郵便の宛先	Post Office Address c/o Mitsubishi Denki Kabushiki Kaisha
	2-3, Marunouchi 2-chome, Chiyoda-ku, TOKYO 100-8310 JAPAN

第4の共同発明者の氏名(該当する場合)	Full name of fourth joint inventor, if any Atsushi HACHISUKA
同第4共同発明者の署名　日付	Fourth Inventor's signature　Date Atsushi Hachisuka　November 18, 1998
住所	Residence Hyogo, Japan
国籍	Citizenship Japanese
郵便の宛先	Post Office Address c/o Mitsubishi Denki Kabushiki Kaisha
	2-3, Marunouchi 2-chome, Chiyoda-ku, TOKYO 100-8310 JAPAN

第5の共同発明者の氏名(該当する場合)	Full name of fifth joint inventor, if any Koji TANIGUCHI
同第5共同発明者の署名　日付	Fifth Inventor's signature　Date Koji Taniguchi　November 18, 1998
住所	Residence Hyogo, Japan
国籍	Citizenship Japanese
郵便の宛先	Post Office Address c/o Mitsubishi Denki Kabushiki Kaisha
	2-3, Marunouchi 2-chome, Chiyoda-ku, TOKYO 100-8310 JAPAN

第6の共同発明者の氏名(該当する場合)	Full name of sixth joint inventor, if any
同第6共同発明者の署名　日付	Sixth Inventor's signature　Date
住所	Residence
国籍	Citizenship
郵便の宛先	Post Office Address

(第7またはそれ以降の共同発明者に対しても同様な情報および署名を提供すること。)

(Supply similar information and signature for seventh and subsequent joint inventors.)

Docket No.: 49657-274 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	
	:	
Eiji HASUNUMA, et al.	:	
	:	
Serial No.:	:	Group Art Unit:
	:	
Filed: January 11, 1999	:	Examiner:
	:	

For: SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEROF

Honorable Commissioner of
Patents and Trademarks
Washington, D. C. 20231

CORRESPONDENCE ADDRESS CHANGE

Sir:

Please change the records to indicate the current firm name and telephone number for the above-identified application and forward all future correspondence as follows:

McDERMOTT, WILL & EMERY
600 13th Street, N.W.
Washington, DC 20005-3096

202-756-8000
Facsimile: 202-756-8087

Respectfully submitted,

MCDERMOTT, WILL & EMERY

Stephen A. Becker
Registration No. 26,527

600 13th Street, N.W.
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Date: January 11, 1999
Facsimile: (202) 756-8699

☒ Please charge my Deposit Account No. 500417 in the amount of $800.00. A duplicate copy of this sheet is enclosed.

☒ The Commissioner is hereby authorized to charge payment of the following fees associated with this communication or credit any overpayment to Deposit Account No. 500417. A duplicate copy is enclosed.

- ☒ Any additional filing fees required under 37 CFR 1.16.

☒ The Commissioner is hereby authorized to charge payment of the following fees during the pendency of this application or credit any overpayment to Deposit Account No. 500417. A duplicate copy of this sheet is enclosed.

- ☒ Any patent application processing fees under 37 CFR 1.17.
- ☒ Any filing fees under 37 CFR 1.16 for presentation of extra claims.

Respectfully submitted,

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